

SMD Crystal Clock Oscillator (SPXO)

1.6 mm x 1.2 mm / 3 MHz to 80 MHz / CMOS / 1.8 V to 3.3 V

FCXO-07

FEATURES

- 1612 size, CMOS crystal clock oscillator (3 MHz to 80 MHz)
- Frequency tolerance of ± 7 ppm (@25 °C) available
- Robust ceramic package with metal lid sealed by electron beam
- RoHS compliant / Lead-free



(1.6 × 1.2 × 0.7 mm)



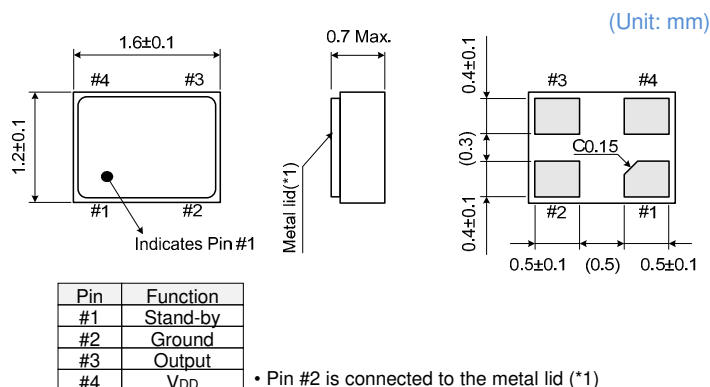
APPLICATIONS

- Mobile communication, wireless-modules

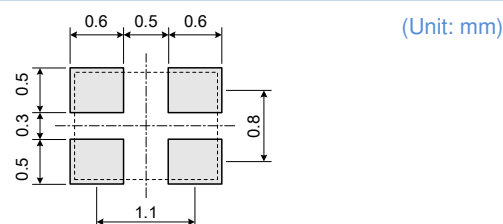
STANDARD SPECIFICATIONS

Item	Specifications	Unit	Conditions (Remarks)
Nominal frequency	3 to 80	MHz	-
Frequency tolerance	± 7	ppm	@25 °C (See below for more options)
Storage temperature	-55 to +125	°C	-
Operating temperature	-40 to +85	°C	(See below for more options)
Frequency / temperature characteristics	± 10 (-30 °C to +85 °C) ± 15 (-40 °C to +85 °C)	ppm	Refer to 25 °C (See below for more options)
Supply voltage	1.8, 3.3	V	(See below for more options)
Current consumption (Max.)	2.0	mA	F = 40 MHz, V _{DD} = 3.0 V, No load
Stand-by current (Max.)	10	μA	Stand-by = "L"
Output voltage	V _{OH} (Min.)	0.9V _{DD}	V I _{OH} = -4 mA
	V _{OL} (Max.)	0.1V _{DD}	V I _{OL} = +4 mA
Output load (Max.)	15	pF	-
Output level	CMOS	-	-
Symmetry (Duty Cycle)	50 ± 5	%	V _{TH} = 0.5V _{DD}
Rise time / Fall time (Max.)	4.5	ns	0.1V _{DD} to 0.9V _{DD}
Start-up time (Max.)	2.0	ms	V _{DD} = 3.3 V
	5.0	ms	V _{DD} = 1.8 V
Random Jitter (Typ.)	2.9	ps	V _{DD} = 3.3 V Measured on WaveCrest 3100C
Total Jitter (Typ.)	40	ps	V _{DD} = 3.3 V, T _J = n°RJ (n ≈ 14.1, BER = 10 ⁻¹²) Measured on WaveCrest 3100C
Phase Noise (Max.)	1.0	ps	V _{DD} = 3.3 V Offset frequency = 12 kHz to 5 MHz
Stand-by function (Pin #1)	V _{IH} (Min.)	0.7V _{DD}	V Output (Pin #3) enabled
	V _{IL} (Max.)	0.3V _{DD}	V Output (Pin #3) disabled = High-Z
Tape and reel	3000	pcs/reel	Reel diameter : \varnothing 180 mm

OUTLINE DIMENSIONS



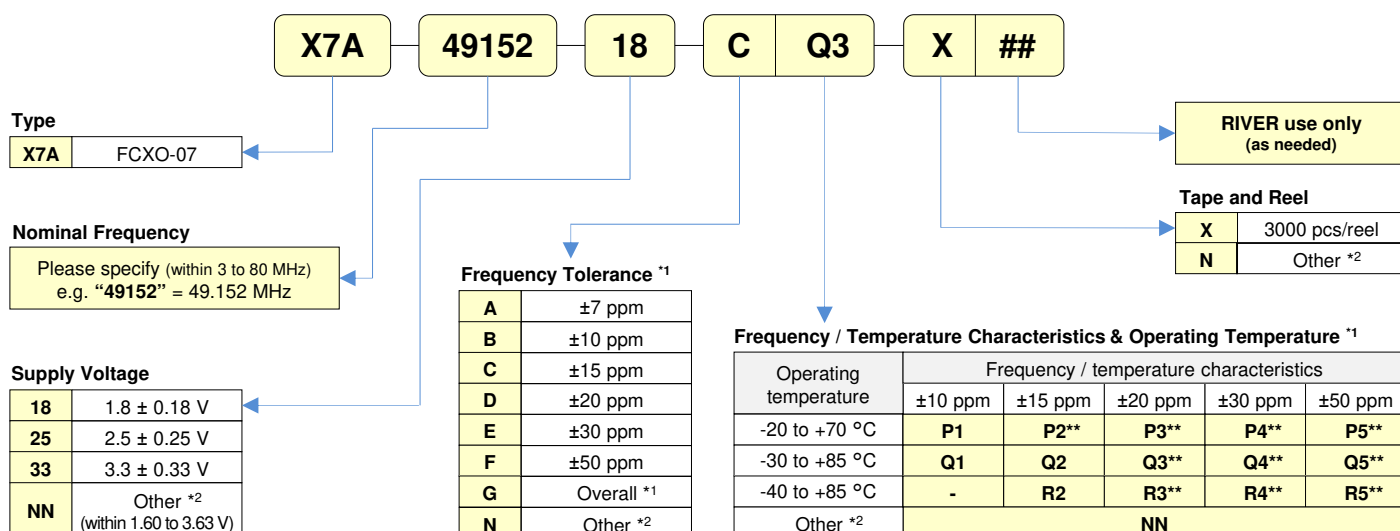
RECOMMENDED LAND PATTERN



GENERAL NOTES

- Certain combinations of standard options may be classified as high-spec models.
- Please consult us for specifications that do not match the standard specifications.
- The information in this document is subject to change without notice.
- For operational stability, a 0.01 μF bypass capacitor should be placed between V_{DD} (Pin #4) and Ground (Pin #2) as close as possible to the product.

ORDERING NUMBER GUIDE



*1. For overall frequency stability inclusive of stability at 25 °C and an operating temp. range, please select "G (Overall)" from the table "Frequency Tolerance" followed by a code that is with " ** " from the table "Freq./Temp. Characteristics & Operating Temp". (e.g. GP2 = Overall ±15 ppm (-20 to +70 °C))

*2. Please consult us for your requirements.

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